Notice of Allowability	Application No.	Applicant(s)	
	10/041,796	CHEUNG ET AL.	
	Examiner	Art Unit	
	Natalia Figueroa	2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendement filed August 11, 2004*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ The drawings filed on *07 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REASONS FOR ALLOWANCE

Allowable Subject Matter

1. Claims 1 through 21 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Regarding claims 1 and 8; the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a system, comprising a gain stage module including a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module.

Regarding claim 21; the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a system, comprising a gain stage module including a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor; a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the drain terminal of the fourth transistor and the gate terminal of the second transistor; and a capacitor coupled between ground and the drain

terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

Regarding claim 2, the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a system, comprising one of the cascode FETS includes a dimension ratio (width/length) with a value of at least 4000.

Regarding claim 3, the prior art of record, and in particular Jusuf et al (USPN 6,219,195), fails to teach or suggest a system, comprising a gain stage module including a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal and a drain terminal coupled to the output of the gain stage module; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor; a first transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the drain terminal of the fourth transistor and the gate terminal of the second transistor; and a capacitor coupled between ground and the drain terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (703) 305-1260. The examiner can normally be reached on Monday - Thursday 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh N. Tran can be reached on (703) 305-4040. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NFM
NFM

Andrew L. Sniezek

ANDREW L. SNIEZEK
PRIMARY EXAMINER